ABSTRACT

An impedance matched write circuit is provided that shunts one or more matching resistors. The impedance matched write circuit includes an interconnect for connecting to a write head and at least one resistor between a control voltage and the interconnect for impedance matching to the interconnect. A transistor can be connected across the resistor to shunt current that would otherwise pass through the resistor during an overshoot mode. The transistor may be a PMOS transistor or a combination of PMOS and NMOS transistors. A gate voltage of the transistor is controlled by a source such that the transistor is turned on in an overshoot mode and turned off during a steady state mode.

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